UNITED STATES PATENT AND TRADEMARK OFFICE

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EXAMINER
UNELUS, ERNEST

ART UNIT	PAPER NUMBER
2181	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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PTOL-90A (Rev. 04/07)

Office Action Summary	Application No.	Applicant(s)
	10/707,871	LIU ET AL.
	Examiner	**Art Unit**
	ERNEST UNELUS	2181

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>30 March 2010</u>.

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>1-4,6,10-22,24-27,30,32-87,90-93,97-101 and 103</u> is/are pending in the application.

    4a) Of the above claim(s) <u>54-77</u> is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) <u>1-4,6,10-22,24-27,30,32-53,78-87,90-93,97-101 and 103</u> is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on <u>20 January 2004</u> is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All   b) ☐ Some *   c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

RESPONSE TO AMENDMENT

Claim rejections based on prior art

A request for continued examination under 37 CFR 1.114, including the fee set forth in

37 CFR 1.17(e), was filed in this application after final rejection. Since this application is

eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e)

has been timely paid, the finality of the previous Office action has been withdrawn pursuant to

37 CFR 1.114. Applicant's submission filed on 03/30/2010 has been entered.

Applicant's arguments filed 03/30/2010 with respect to claims 1-4, 6, 10-22, 24-27, 30,

32-53, 78-87, 90-93, 97-101, and 103 have been fully considered but are moot in view of the

new ground(s) of rejection.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

1.   The applicant's oath/declaration has been reviewed by the examiner and is found to

conform to the requirements prescribed in **37 C.F.R. 1.63.**

INFORMATION CONCERNING DRAWINGS

Drawings

2.   The applicant's drawings submitted are acceptable for examination purposes.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

3.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4.   **Claims 1-4, 6, 10, 12-17, 19-22, 24, 26-27, 30, 32-38, 40-46, 50, 78-83, 86-87, 90-93,**

97-101, and 103, are rejected under 35 U.S.C. 103(a) as being unpatentable over Bicknell et al.

(US pub. 2003/0193776) in view of Meehan et al. (US pub. 2004/0177218) and in further view

of Guha et al. (US pub. 2006/0129761).

5.   As per **claims 1, 21, 78, and 90**, Bicknell discloses "A storage virtualization computer

system **(system 100 of fig. 6)** comprising:

a host entity for issuing IO requests **(Host computer of fig. 6)**;

an external storage virtualization controller **(controller 1)** coupled to said host entity for

executing IO operations in response to said IO requests **(see fig. 6 and paragraph 0029)**; and

a group of physical storage devices (PSDs) **(Discs in the disc pack 118 of the spindle**

motor of disc drive 106, as discloses in paragraph 0018; see also figs. 3 and 6. A group of

PSDs, for example, is four discs in two separate disc packs 118 in two separate disc drives

106), each coupled to the external storage virtualization controller through a point-to-point

serial-signal interconnect **(see fig. 6 and paragraph 0019)**, for providing storage to the storage

virtualization computer system through the external storage virtualization controller **(see**

paragraph 0027),

wherein said computer system further comprises a detachable canister **(housing 116 of fig. 3, as discloses in para. 0018)** attached to said external storage virtualization controller for containing one of said at least one PSDs therein **(see fig. 2 and see paragraph 0019, which discloses "Disc drive 106 can preferably be removed without disturbing the operation of subsystem 100")**;

wherein said external storage virtualization controller is configured to define at least one logical media unit (LMU) **(a spindle motor having disc pack 118 of fig. 3, as discloses in para. 0018. a logical media unit is not a well-know term in the art)** consisting of sections of at least one said group of PSDs **(see fig. 2 and see paragraph 0018. a group of PSD is a group of disk in a spindle)**.

but fails to disclose expressly "wherein said external storage virtualization controller comprises: a central processing circuitry for performing said IO operations in response to said IO requests of said host entity;

at least one IO device interconnect controller coupled to said central processing circuitry;

at least one host-side IO device interconnect port provided in one of said at least one IO device interconnect controller for coupling to said host entity; and

at least one device-side IO device interconnect port provided in one of said at least one IO device interconnect controller for coupled to said group of PSDs through said point-to-point serial-signal interconnect, said device-side IO device interconnect port being a serial port for point-to-point serial-signal transmission; and

wherein said external SVC issues a device-side IO request to said IO device interconnect controller, and said IO device interconnect controller re-formats said device-side IO request and

accompanying IO data into at least one data packet for transmission to said group of PSDs

through said device-side IO device interconnect port".

Meehan discloses "wherein said external storage virtualization controller comprises: a

central processing circuitry **(microprocessor 406 of fig. 6, as discloses in para. 0028)** for

performing said IO operations in response to said IO requests of said host entity **(see fig. 5 and**

para. 0028);

at least one IO device interconnect controller **(FPGA 409 of fig. 6, as discloses in para.**

0028) coupled to said central processing circuitry **(see fig. 6)**;

at least one host-side IO device interconnect port **("host interface 411 (from the host)",**

as discloses in para. 0029) provided in one of said at least one IO device interconnect controller

for coupling to said host entity **(see para. 0029, which discloses "Data to be written to storage**

disks 401-404 would move from the host interface 411 (from the host), optionally through a

primary RAID Controller (if present), through the Interface connector 410, and into the

buffer RAM 407 of RAID Controller 400"); and

at least one device-side IO device interconnect port **("interface 411", as discloses in**

para. 0029) provided in one of said at least one IO device interconnect controller for coupled to

one of said at least one physical storage device through said point-to-point serial-signal

interconnect **(see para. 0029 and fig. 6, which show the interface 411 as part of the**

controller; in other words, the drawing illustrated part of the interface 411 is inside the

controller. See para. 0029 and fig. 6 for SAS transmission and point-to-point serial-signal

interconnect), said device-side IO device interconnect port being a serial port for point-to-point

serial-signal transmission **(See para. 0029 and fig. 6 for SAS transmission and point-to-point serial-signal interconnect)**; and

wherein said external SVC issues a device-side IO request to said IO device interconnect controller, and said IO device interconnect controller re-formats said device-side IO request and accompanying IO data into at least one data packet for transmission to said PSD through said device-side IO device interconnect port" **(see para. 0029, which discloses the FPGA 409 'manipulating' data between the host and the storage devices. Manipulating is a form of 're-formatting'. The claim language is not specific as to how this reformatting is being done. See also para. 0016, which discloses 're-distributed' the data).**

Neither Bicknell nor Meehan specifically discloses a logical media unit that is configured to provide a mapping that maps combination of the sections of said group of PSDs to the at least one LMU visible to the host entity, and the at least one LMU is contiguously addressable by the host entity to which the at least one LMU is made available; and wherein a new PSD is attached to said external storage virtualization controller when said external storage virtualization controller is on-line.

Guha discloses a logical media unit that is configured to provide a mapping that maps combination of the sections of said group of PSDs to the at least one LMU visible to the host entity, and the at least one LMU is contiguously addressable by the host entity to which the at least one LMU is made available **(paragraph 0018 of Bicknell discloses, "Disc drive 106 also includes a disc pack 118, which is mounted on a spindle motor (not shown) by a disc clamp 120"; similarly, see paragraph 0132 of Guha, which discloses, "the single drives described above can each be representative of a set of disk drives. This disk drive configuration**

could comprise RAID10 or some form of data organization that would "spread" a hot spot over many disk drives (spindles). Set of Disk Drives becoming Redundant", and paragraph 0129, which discloses to contiguously address those disk drives); and wherein a new PSD is attached to said external storage virtualization controller when said external storage virtualization controller is on-line **(see paragraph 00138)**.

Bicknell et al. (US pub. 2003/0193776), Meehan et al. (US pub. 2004/0177218), and Guha et al. (US pub. 2006/0129761) are analogous art because they are from the same field of endeavor of redundant array of independent disks (RAID) architectures.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a disc storage subsystem that allows continued access to data stored in its Advanced Technology Architecture (ATA) disc drives in the event of a controller failure as described by Bicknell, a redundant array of independent disks (RAID) architectures, and more specifically, to a multiple level RAID architecture as taught by Meehan, and a large number of hard disk drives that are individually controlled, so that only the disk drives that are in use are powered on as described by Guha.

The motivation for doing so would have been because Meehan teaches that a RAID stripe can be use to write data to multiple storage devices at the same time, which allows the data to be evenly written and maximize overall system performance (see paragraph 0006).

The motivation for doing so would have been because Guha teaches that keeping on only the drives that are in use saves power, which takes place through addressing each disk drive (see paragraph 0026).

Therefore, it would have been obvious to combine Guha et al. (US pub. 2006/0129761),

Meehan et al. (US pub. 2004/0177218), and Bicknell et al. (US pub. 2003/0193776) for the

benefit of creating the computer system to obtain the invention as specified in claims 1, 21, 78,

and 90.

6.   As per **claims 2, 22, 79, and 91**, the combination of Bicknell, Meehan, and Guha

discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses

wherein said point-to-point serial-signal interconnect is a Serial ATA IO device interconnect **(see

fig.6 and paragraph 0019).**

7.   As per **claims 3, 26, 86, and 92**, the combination of Bicknell, Meehan, and Guha

discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses

wherein a said group of PSDs comprises a SATA PSD **(see paragraph 0019).**

8.   As per **claims 4, 30, 87, and 93**, the combination of Bicknell, Meehan, and Guha

discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses

wherein a said group PSDs comprises a PATA PSD and a serial-to-parallel converter **(data

interface 144 of fig. 6)** is provided between said device-side IO device interconnect controller

and said PATA PSD **(see paragraph 0030).**

9.   As per **claims 6 and 32**, the combination of Bicknell, Meehan, and Guha discloses "The

computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein one of

said PSDs can be detached from said external storage virtualization controller when said external

storage virtualization controller is on-line **(see paragraph 0019, which discloses "Disc drive 106 can preferably be removed without disturbing the operation of subsystem 100")**.

10.   As per **claim 33**, the combination of Bicknell, Meehan, and Guha discloses "The storage virtualization subsystem of claim 21" **[See rejection to claim 21 above]** Bicknell discloses wherein said a new PSD can be attached to said external storage virtualization controller when said external storage virtualization controller is on-line **(see paragraph 0030).**

11.   As per **claims 10 and 24**, the combination of Bicknell, Meehan, and Guha discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Meehan discloses wherein a said host-side IO device interconnect port and a said device-side IO device interconnect port are provided in the same IO device interconnect controller **(see para. 0029 and fig. 6).**

12.   As per **claims 12 and 27**, the combination of Bicknell, Meehan, and Guha discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein said storage virtualization controller comprises a plurality of host-side IO device interconnect ports each for coupling to a host-side IO device interconnect **(see fig. 6 and paragraph 0026).**

13.   As per **claim 13**, the combination of Bicknell, Meehan, and Guha discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein said external storage virtualization controller is configured to present redundantly the at least one

LMU through at least two of said plurality of host-side IO device interconnect ports **(see paragraphs 0018 and 0019).**

14.   As per **claims 14 and 35**, the combination of Bicknell, Meehan, and Guha discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein at least one said host-side IO device interconnect port is Fibre Channel supporting point-to-point connectivity in target mode **(see paragraph 0030 and fig. 6).**

15.   As per **claims 15 and 36**, the combination of Bicknell, Meehan, and Guha discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein at least one said host-side IO device interconnect port is Fibre Channel supporting private loop connectivity in target mode **(see paragraph 0030 and fig. 6).**

16.   As per **claims 16 and 37**, the combination of Bicknell, Meehan, and Guha discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein at least one said host-side IO device interconnect port is Fibre Channel supporting public loop connectivity in target mode **(see paragraph 0032 and fig. 6).**

17.   As per **claims 17 and 38**, the combination of Bicknell, Meehan, and Guha discloses "The computer system of claim 1," **[See rejection to claim 23 above]**, Meehan discloses wherein at least one said host-side IO device interconnect port is parallel SCSI operating in target mode **(see paragraph 0029).**

18.   As per **claims 19 and 40**, the combination of Bicknell, Meehan, and Guha discloses "The

computer system of claim 1," **[See rejection to claim 23 above]**, Meehan discloses wherein at

least one said host-side IO device interconnect port is Serial-Attached SCSI (SAS) operating in

target mode **(see paragraph 0029)**.

19.   As per **claims 20 and 41**, the combination of Bicknell, Meehan, and Guha discloses "The

computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein at

least one said host-side IO device interconnect port is Serial ATA operating in target mode **(see

paragraph 0019)**.

20.   As per **claims 34, 101, and 103**, the combination of Bicknell, Meehan, and Guha

discloses "The virtualization subsystem of claim 21" **[See rejection to claim 21 above]** Bicknell

discloses wherein said group of PSDs include a first set of PSDs and a second set of PSDs, said

first set of PSDs and said second set of PSDs are not received in a same enclosure **(see figures 3

and 6)**, and said storage virtualization controller further comprises at least one multiple-device

device-side expansion port **(Midplane Card ports 209 of fig. 6)** for coupling to said second

set of said PSDs **(see fig. 6)**.

21.   As per **claims 42 and 80**, the combination of Bicknell, Meehan, and Guha discloses "The

virtualization subsystem of claim 21" **[See rejection to claim 21 above]** Bicknell discloses

comprising an enclosure management services mechanism **(interface 200, as discloses in paragraph 0024 and fig. 1)**.

22.   As per **claim 43**, the combination of Bicknell, Meehan, and Guha discloses "The virtualization subsystem of claim 42" **[See rejection to claim 42 above]** Bicknell discloses wherein said enclosure management services mechanism manages and monitors <u>at least one</u> of the following devices belonging to the storage virtualization subsystem: power supplies, fans, temperature sensors, voltages, uninterruptible power supplies, batteries, LEDs, audible alarms, PSD canister locks, door locks **(see paragraph 0031)**.

23.   As per **claim 44**, the combination of Bicknell, Meehan, and Guha discloses "The virtualization subsystem of claim 42" **[See rejection to claim 42 above]** Bicknell discloses wherein said enclosure management services mechanism is configured to support direct-connect EMS configuration **(see fig. 8)**.

24.   As per **claim 45**, the combination of Bicknell, Meehan, and Guha discloses "The virtualization subsystem of claim 42" **[See rejection to claim 42 above]** Bicknell discloses wherein said enclosure management services mechanism is configured to support device-forwarded EMS configuration **(see fig. 8)**.

25.   As per **claims 46, 81, 82, and 83**, the combination of Bicknell, Meehan, and Guha discloses "The virtualization subsystem of claim 42" **[See rejection to claim 42 above]** Bicknell

discloses wherein said enclosure management services mechanism is configured to support direct-connect EMS configuration and device-forwarded EMS configuration **(see fig. 2)**.

26.   As per **claim 50**, the combination of Bicknell, Meehan, and Guha discloses "The virtualization subsystem of claim 42" **[See rejection to claim 42 above]** Bicknell discloses wherein said EMS mechanism further comprises status-monitoring circuitry to communicate with said external storage virtualization controller **(see paragraph 0031)**.

27.   As per **claims 97-100**, the combination of Bicknell, Meehan, and Guha discloses "The storage computer system of claim 1" **[See rejection to claim 42 above]** Bicknell discloses wherein said group of PSDs are received in a plurality of enclosures **(see figures 3 and 6)**.

28.   **Claims 11 and 25,** are rejected under 35 U.S.C. 103(a) as being unpatentable over Bicknell et al. (US pub. 2003/0193776) in view of Meehan et al. (US pub. 2004/0177218) and Guha et al. (US pub. 2006/0129761) as applied to claim 1 above, and further in view of Otterness et al. (US pub. 2002/0152355).

29.   As per **claims 11 and 25,** the combination of Bicknell, Meehan, and Guha discloses "The storage virtualization computer system of claim 1," **[See rejection to claim 1 above]**, but fails to disclose expressly wherein said at least one IO device interconnect controller comprises a plurality of IO device interconnect controller; wherein said host-side I0 device interconnect port

and said device-side IO device interconnect port are provided in different said IO device

interconnect controllers.

Otterness discloses "wherein said at least one IO device interconnect controller comprises

a plurality of IO device interconnect controller; wherein said host-side IO device interconnect

port and said device-side IO device interconnect port are provided in different said IO device

interconnect controllers" **(see fig. 4, which discloses a controller such as a RAID controller**

199 having a processor 216 such as the 'central processing circuit' as claimed. Fig. 4 also

discloses multiple processor/memory controllers 204 and 206 connected to the processor

216. Multiple processor/memory controllers 204 and 206 are shown to have their own

device port and host port. See para. 0048 for more detail).

Bicknell et al. (US pub. 2003/0193776), Meehan et al. (US pub. 2004/0177218), Guha et

al. (US pub. 2006/0129761), and Otterness et al. (US pub. 2002/0152355) are analogous art

because they are from the same field of endeavor of redundant array of independent disks

(RAID) architectures.

At the time of the invention it would have been obvious to a person of ordinary skill in

the art to modify a disc storage subsystem that allows continued access to data stored in its

Advanced Technology Architecture (ATA) disc drives in the event of a controller failure as

described by Bicknell, a redundant array of independent disks (RAID) architectures, and more

specifically, to a multiple level RAID architecture as taught by Meehan, a large number of hard

disk drives that are individually controlled, so that only the disk drives that are in use are

powered on as described by Guha, and device interconnection topologies, and methods for

communicating data or other information between such devices; more particularly to inter- and

intra-device connection and communication topologies and methods for such communication; and most particularly to RAID storage system controllers that increase available storage device interconnect channel capacity by routing controller-to-controller messages to a communication channel separate from the communication channel normally used to communicate the RAID data as taught by Otterness.

The motivation for doing so would have been because Otterness teaches that"

Embodiments of the NorthBay.TM. provides support services for a RAID controller. Among other things, the NorthBay ASIC implements a fast special-purpose-processor that computes the parity values used in the RAID system. The data for which the NorthBay ASIC is to handle memory operations and compute parity is specified by the RAID controller's CPU in response to host disk transactions" (see paragraph 0018).

Therefore, it would have been obvious to combine Otterness et al. (US pub. 2002/0152355) with Meehan et al. (US pub. 2004/0177218), Bicknell et al. (US pub. 2003/0193776), and Guha et al. (US pub. 2006/0129761) for the benefit of creating the storage virtualization computer system to obtain the invention as specified in claims 11 and 25.

30.   **Claims 47, 48, 84, and 85**, are rejected under 35 U.S.C. 103(a) as being unpatentable over Bicknell et al. (US pub. 2003/0193776) in view of Meehan et al. (US pub. 2004/0177218) and Guha et al. (US pub. 2006/0129761) as applied to claim 1 above, and further in view of Rabinovitz et al. (US pat. 6,483,107).

31.   As per **claims 47 and 84**, the combination of Bicknell, Meehan, and Guha "The storage

virtualization subsystem of claim 42," **[See rejection to claim 42 above]**, including the

enclosure management services mechanism, but fails to disclose expressly wherein said

enclosure management services mechanism is configured to support SES enclosure management

services protocol.

Rabinovitz discloses a SES in a storage virtualization subsystem **(col. 17, line 23).**

Bicknell et al. (US pub. 2003/0193776), Meehan et al. (US pub. 2004/0177218), Guha et

al. (US pub. 2006/0129761), and Rabinovitz et al. (US pat. 6,483,107) are analogous art because

they are from the same field of endeavor of peripheral storage devices.

At the time of the invention it would have been obvious to a person of ordinary skill in

the art to modify a disc storage subsystem that allows continued access to data stored in its

Advanced Technology Architecture (ATA) disc drives in the event of a controller failure as

described by Bicknell, a redundant array of independent disks (RAID) architectures, and more

specifically, to a multiple level RAID architecture as taught by Meehan, a large number of hard

disk drives that are individually controlled, so that only the disk drives that are in use are

powered on as described by Guha, and a canister and a casing of a computer peripheral enclosure

as taught by Rabinovitz.

The motivation for doing so would have been because Rabinovitz teaches that a SES

allow a user to monitor the enclosure from a remote location **(see col. 17, lines 29-31).**

Therefore, it would have been obvious to combine Rabinovitz et al. (US pat. 6,483,107)

with Bicknell et al. (US pub. 2003/0193776), Meehan et al. (US pub. 2004/0177218), and Guha

et al. (US pub. 2006/0129761) for the benefit of creating the storage virtualization subsystem to

obtain the invention as specified in claims 47 and 84.

32.   As per **claims 48 and 85**, the combination of Bicknell, Meehan, Guha, and Rabinovitz

discloses "The storage virtualization subsystem of claim 42," **[See rejection to claim 42 above]**

Bicknell discloses the enclosure management services mechanism, and Rabinivitz further

discloses the SAF-TE, **(see col. 17, line 29).**

33.   **Claims 18, 39, 49, 51, 52, and 53**, are rejected under 35 U.S.C. 103(a) as being

unpatentable over Bicknell et al. (US pub. 2003/0193776) in view of Meehan et al. (US pub.

2004/0177218) and Guha et al. (US pub. 2006/0129761), as applied to claim 1 above, and further

in view of Colton (US pub. 2005/0089027).

34.   As per **claims 18 and 39**, the combination of Bicknell, Meehan and Guha, discloses "The

computer system of claim 1," **[See rejection to claim 1 above]**, including at least one said host-

side IO device interconnect port **(see fig. 6)**, but fails to disclose expressly wherein at least one

said host-side IO device interconnect port is ethernet supporting the iSCSI protocol operating in

target mode.

        Colton discloses ethernet supporting the iSCSI protocol operating in target mode **(see fig.**

11 and paragraph 1487, which discloses internet SCSI in an Ethernet network).

        Bicknell et al. (US pub. 2003/0193776), Meehan et al. (US pub. 2004/0177218), Guha et

al. (US pub. 2006/0129761), and Colton (US pub. 2005/0089027) are analogous art because they

are from the same field of endeavor of data transfer.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a disc storage subsystem that allows continued access to data stored in its Advanced Technology Architecture (ATA) disc drives in the event of a controller failure as described by Bicknell, a redundant array of independent disks (RAID) architectures, and more specifically, to a multiple level RAID architecture as taught by Meehan, a large number of hard disk drives that are individually controlled, so that only the disk drives that are in use are powered on as described by Guha, and a system and method for transferring data optically via an intelligent optical switching network as taught by Colton.

The motivation for doing so would have been because Colton teaches that **"The Sun server(s) running Oracle should have a minimum of 2 high-speed SCSI disk drives to ensure adequate performance" (see paragraph 1487).**

Therefore, it would have been obvious to combine Colton (US pub. 2005/0089027) with Bicknell et al. (US pub. 2003/0193776), Meehan et al. (US pub. 2004/0177218), and Guha et al. (US pub. 2006/0129761) for the benefit of creating the computer system to obtain the invention as specified in claims 18 and 39.

35.   As per **claims 49, 51, and 53**, the combination of Bicknell, Meehan, Guha and Colon discloses "The storage virtualization subsystem of claim 42," **[See rejection to claim 42 above]** Bicknell discloses the enclosure management services mechanism and <u>an</u> external storage virtualization controller **(see fig. 2)**, and Colon further discloses 12C latches, **(see fig. 11).**

36.   As per **claim 52**, the combination of Bicknell, Meehan, Guha and Colon discloses "The storage virtualization subsystem of claim 42," **[See rejection to claim 42 above]** Bicknell

discloses the enclosure management services mechanism as a micro-computer **(see fig. 2)**, and

Colon further discloses a CPU for running a program, **(see paragraph 0810 and fig. 11).**

RELEVANT ART CITED BY THE EXAMINER

37.   The following prior art made of record and not relied upon is cited to establish the level

of skill in the applicant's art and those arts considered reasonably pertinent to applicant's

disclosure. See **MPEP 707.05(c)**.

38.   The following reference teaches a storage virtualization computer system.

U.S. PATENT NUMBER

US 2002/0144044; 6,845,428; 6,178,520

CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as

recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-4, 6, 10-22, 24-27, 30, 32-53, 78-87, 90-93, 97-101,

and 103 have received a first action on the merits and are subject of a first action non-final.

DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Ernest Unelus whose telephone number is (571) 272-

8596. The examiner can normally be reached on Monday to Friday 9:00 AM to 5:00 PM.

<u>IMPORTANT NOTE</u>

If attempts to reach the above noted Examiner by telephone are unsuccessful,

the Examiner's supervisor, Mr. Alford Kindred, can be reached at the following telephone

number: Area Code (571) 272-4037.

The fax phone number for the organization where this application or proceeding

is assigned is 571-273-8300. Information regarding the status of an application may be

obtained from the Patent Application Information Retrieval (PAIR) system. Status

information for published applications may be obtained from either Private PAIR or

Public PAIR. Status information for unpublished applications is available through Private

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Should you have questions on access to the Private PAIR system, contact the

Electronic Business Center (EBC) at 866-217- 91 97 (toll-free).

July 22, 2010

/E. U./
Examiner, Art Unit 2181

/Chun-Kuan Lee/
Primary Examiner, Art Unit 2181

Ernest Unelus
Patent Examiner
Art Unit 2181